AMENDMENTS TO THE CLAIMS

Please amend claim 27 as follows.

1. (Previously presented) A circuit, comprising:

a first control register to be loadable after the circuit is reset, the first control register to store data that describes an operational mode of the circuit;

a first plurality of control registers to be loadable during an initialization process after the circuit is reset and to be unloadable until the circuit is reset again, the first plurality of control registers to store sensitive data based on different operational modes of the circuit; and

a first switch unit coupled to the first control register and the first plurality of control registers, wherein the first switch unit to output sensitive data stored by one control register of the first plurality of control registers based on the data loaded in the first control register and to output sensitive data stored by another control register of the first plurality of control registers based on different data loaded in the first control register, the different data loaded in response to a change in the circuit's operational mode, the sensitive data to be used by a unit coupled to the circuit, the unit to operate in accordance with the sensitive data to prevent damage to the circuit.

2. (Original) The circuit of claim 1, wherein the first switch unit comprises a multiplexer having input ports coupled to receive output from the first plurality of control registers and having a control port coupled to receive output from the first control register.

3. (Original) The circuit of claim 1, wherein the first control register is loadable through software control after the circuit is reset.

4. (Previously presented) The circuit of claim 3, wherein the software control to cause the first control register to be loaded with different data in response to the change in the circuit's operational mode.

5. (Original) The circuit of claim 1, wherein the circuit is a memory controller.

6. (Original) The circuit of claim 1, wherein the first plurality of control registers to be loaded by a basic input output system (BIOS) during an initialization process after the circuit is reset.

7. (Original) The circuit of claim 6, wherein the first plurality of control registers to be locked by the BIOS during the initialization process after the circuit is reset.

8. (Original) The circuit of claim 7, wherein the first plurality of control registers each include a lock bit to be set by the BIOS to lock the first plurality of control registers during the initialization process after the circuit is reset.

9. (Previously presented) The circuit of claim 1, further comprising:

a second control register to be loadable after the circuit is reset;

a second plurality of control registers to be loadable during the initialization process and to be unloadable until the circuit is reset again; and

a second switch unit coupled to the second control register and the second plurality of control registers, wherein the second switch unit to output data stored by one control register of the second plurality of control registers based on the data loaded in the second control register.

Claims 10-16 (Cancelled)

17. (Previously presented) A method, comprising:

storing first data and second data in a circuit, the second data including a plurality of portions, wherein, after the circuit is reset and initialized, the first data is changeable and the second data is not changeable, the first data describing an operational mode of the circuit;

selecting one portion of the plurality of portions in response to the first data, wherein the selected portion to be provided to a unit of the circuit, the unit to operate in accordance with the one portion to prevent damage to the circuit;

changing the first data in response to a change in the circuit's operational mode; and

selecting another portion of the plurality of portions in response to the change in the first data, the unit to operate in accordance with the another portion to prevent damage to the circuit.

18. (Previously presented) The method of claim 17, wherein the first data is changed in response to software control.

19. (Previously presented) The method of claim 17, wherein the unit includes at least one of a thermal control unit and a power conservation unit.

20. (Previously presented) The method of claim 17, wherein storing second data comprises:

storing the second data by a basic input output system (BIOS) while the circuit is initialized.

21. (Previously presented) The method of claim 20, wherein the BIOS locks one or more control registers storing second data to prevent changes to the second data after the circuit is initialized.

22. (Previously presented) A method, comprising:

loading a plurality of control registers of a circuit, the plurality of control registers including a plurality of protected control registers and unprotected control registers, wherein the plurality of protected control registers are loaded with sensitive data for use by a unit of the circuit, the unit to operate in accordance with the sensitive data to prevent damage to the circuit;

locking the plurality of protected control registers;

selecting a locked protected control register of the plurality of protected control registers based on an operational mode of the circuit;

outputting the sensitive data stored by the selected locked protected control register to the unit;

deselecting the locked protected control register; and

selecting another locked protected control register of the plurality of protected control registers based on a change in the operational mode of the circuit.

23. (Previously presented) The method of claim 22, wherein the operational mode is described by data stored in an unprotected control register of the plurality of unprotected control registers.

24. (Previously presented) The method of claim 22, wherein the unit includes at least one of a thermal control unit and a power conservation unit.

25. (Previously presented) A circuit, comprising:

a plurality of control registers;

means for loading the plurality of control registers, the plurality of control registers including a plurality of protected control registers and unprotected control registers, wherein the plurality of protected control registers are loaded with sensitive data for use by a unit of the circuit, the unit to operate in accordance with the sensitive data to prevent damage to the circuit;

means for locking the plurality of protected control registers;

means for selecting a locked protected control register of the plurality of protected control registers based on an operational mode of the circuit;

means for outputting the sensitive data stored by the selected locked protected control register to the unit;

means for deselecting the locked protected control register; and

means for selecting another locked protected control register of the plurality of protected control registers based on a change in the operational mode of the circuit.

26. (Previously presented) The circuit of claim 25 wherein the operational mode is described by data stored in an unprotected control register of the plurality of unprotected control registers.

27. (Currently amended) The ~~method~~ circuit of claim 25, wherein the unit includes at least one of a thermal control unit and a power conservation unit.

28. (Prevously presented) A system, comprising:

a processor;

a memory; and

a memory controller coupled to the processor and the memory, the memory controller comprising:

a first control register to be loadable after the memory controller is reset, the first control register to store data that describes an operational mode of the memory controller;

a first plurality of control registers to be loadable during an initialization process after the memory controller is reset and to be unloadable after initialization until the circuit is reset again, the first plurality of control registers to store sensitive data based on different operational modes of the memory controller; and

a first switch unit coupled to the first control register and the first plurality of control registers, wherein the first switch unit to output sensitive data stored by one control register of the first plurality of control registers based on the data loaded in the first control register and to output sensitive data stored by another control register of the first plurality of control registers based on different data loaded in the first control register, the different data loaded in response to a change in the memory controller's operational mode, the sensitive data to be used by a unit coupled to the memory controller, the unit to operate in accordance with the sensitive data to prevent damage to the memory controller.

29. (Original) The system of claim 28, wherein the first switch unit comprises a multiplexer having input ports coupled to receive output from the first plurality of control registers and having a control port coupled to receive output from the first control register.

30. (Previously presented) The system of claim 28, wherein the first control register is loadable in response to software control after the memory controller is initialized.

31. (Previously presented) The method of claim 22, wherein the change in the operational mode is in response to a user input.

32. (Previously presented) The circuit of claim 1, wherein the unit includes at least one of a thermal control unit and a power conservation unit.

33. (Previously presented) A circuit, comprising:

a first multiplexer including a first plurality of input ports, a first output port, and a first control port;

a first non-protected control register coupled to the first control port, the first non-protected control register to be loadable after the circuit is reset, the first control register to store data that describes an operational mode of the circuit;

a first plurality of protected control registers coupled to the first plurality of input ports, the first plurality of protected control registers to be loadable during an initialization process after the circuit is reset and to be unloadable until the circuit is reset again, the first plurality of control registers to store sensitive data based on different operational modes of the circuit,

wherein the first multiplexer to output sensitive data stored in one protected control register of the first plurality of protected control registers in response to the data stored in the first non-protected control register and to output sensitive data stored by another protected control register of the first plurality of protected control registers based on different data loaded in the first non-protected control register, the different data loaded in response to a change in the circuit's operational mode; and

a unit coupled to the first output port of the first multiplexer, the unit to operate in accordance with the sensitive data outputted by the first multiplexer to prevent damage to the circuit.

34. (Previously presented) The circuit of claim 33, further comprising:

a second multiplexer including a second plurality of input ports, a second output port, and a second control port;

a second non-protected control register coupled to the second control port, the second non-protected control register to be loadable after the circuit is reset; and

a second plurality of protected control registers coupled to the second plurality of input ports, the second plurality of protected control registers to be loadable during an initialization process after the circuit is reset and to be unloadable until the circuit is reset again, wherein the second multiplexer to output data stored in one protected control register of the second plurality of protected control registers in response to data stored in the second non-protected control register,

wherein the unit is coupled to the second output port of the second multiplexer, the unit to operate in accordance with the data outputted by the second multiplexer.

35. (Previously presented) The circuit of claim 33, wherein the unit includes at least one of a thermal control unit and a power conservation unit, and wherein the circuit includes a memory controller.

36. (Previously presented) The method of claim 22, wherein the circuit is a memory controller.

37. (Previously presented) The method of claim 22, wherein damage to the circuit includes degraded performance of the circuit.